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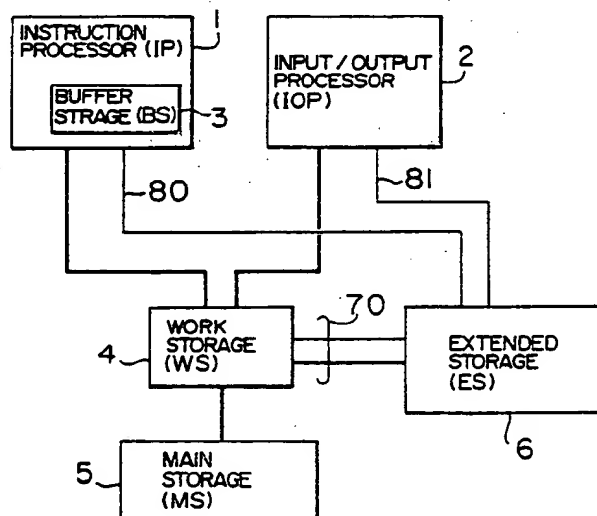
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DE FR GB(71) Applicant: HITACHI, LTD.
6, Kanda Surugadai 4-chome
Chiyoda-ku Tokyo 101(JP)(72) Inventor: Kiriu, Yoshio
2-2-501, Minamigaoka-2-chome
Hadano-shi(JP)(74) Representative: Patentanwälte Beetz sen. -
Beetz jun. Timpe - Siegfried -
Schmitt-Fumian- Mayr
Steinsdorfstrasse 10
D-8000 München 22(DE)

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(54) Extended storage system.

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FIG. 1



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EXTENDED STORAGE SYSTEM

BACKGROUND OF THE INVENTION

This invention relates to an extended storage system for a data processing system, and particularly to an extended storage system suited to transfer data between hierarchical storages and an extended storage.

U.S. Patent No. 4,476,524 issued to D.T. Braun et al. on October 9, 1984 discloses a data processing system which includes a data transfer path between a main storage (will be termed MS hereinafter) and an extended storage (or page storage) and performs data transfer between the MS and extended storage using the data transfer path.

As a prior art for improving the adjustment of difference in the operating speed between the processor and MS in a data processing system, JP-A-52-71138 (corresponding to JP-B-57-57782) discloses hierarchical storages in which a small-capacity, high-speed high ranking storage, e.g., a buffer storage (will be termed BS hereinafter) is provided on the part of the processor, and an intermediate-rank storage, e.g., a work storage (will be termed WS hereinafter) serving as a second-rank buffer, having an intermediate speed and intermediate capacity as compared with the BS and MS is provided between the BS and MS. In this case, the MS is the lowest-rank storage.

U.S. Patent No. 4,639,862 issued to H. Wada on January 27, 1987 discloses an addressing system for the extended storage. The contents of the above publication are introduced to the present patent application without mentioning specifically.

In reading out data such as an instructions or operand stored in three or more hierarchical storages, the data is read out from a storage of as high rank as possible which holds the object data or contains a copy of the data. Only if any storage higher in rank than MS does not contain a copy of data, it is read out from the MS. Control is made to memorize data of much usage at a higher rank storage. The processing speed is thus enhanced.

In writing data into hierarchical storages, data in storages of all ranks are not rewritten at once, but instead altered data is rewritten in a store-in manner for storages below a certain rank. The processing speed is thus enhanced.

Among control modes of rewriting data in a storage of a certain rank, rewriting data immediately, after rewriting data in the certain rank storage, to the next lower ranking storage in categorized to be "store-through" mode, while rewriting data by returning the data to the next lower ranking storage when the rewritten data in the active storage is no longer used is categorized to be "store-

in" mode. In a hierarchical storage system which controls storing into an intermediate storage in store-in mode, the MS which is the lowest-rank storage does not necessarily have its data always updated to the newest state.

Recent advanced semiconductor technologies have provided higher operating speeds for processors, year after year, whereas MSs have been rendered little progress in the operating speed although their capacities have been increased and their costs lowered. Therefore, the difference of speed between these devices is further increasing.

In the data processing system disclosed in the above-mentioned U.S. Patent No. 4,476,524, central processors (CPs) and channel processors (CHs) are connected through a system controller (SC) to main storages (MSs), which are connected with page storages (PSs) through an MS/PS data bus.

SUMMARY OF THE INVENTION

An object of this invention is to provide an extended storage system used suitably for transferring data between hierarchical storages of three ranks or more and an extended storage.

Another object of this invention is to provide an extended storage system which ensures the latest version of copied data by merely having means which, following a data transfer from an extended storage to hierarchical storages, invalidates the copy of transfer destination data among data copied in a storage higher in rank than at least one intermediate-rank storage.

A further object of this invention is to prevent improper data transfer to the ES from the MS whose contents would not be yet updated to the latest version due to the presence of an intermediate-rank work storage which is controlled in store-in mode and is higher in rank than the MS.

A further object of this invention is to solve such a problem that, in case of data transfer from the ES to MS and in case that WS or BS higher in rank than the MS has a copy of data that has been stored in the MS until the transfer, the copied data in the WS or BS is inconsistent with the newly transferred data to the MS and the transferred data solely becomes new data.

According to this invention, the above objectives are achieved through the provision, between at least one intermediate-rank storage controlled in store-in mode and an ES, of a data transfer path for the data transfer between the intermediate-rank storage and the ES, and means of invalidating

transfer destination data of the data to be transferred in the hierarchical storages, i.e., portion corresponding to the data to be cancelled because of change in destined portion, among data copied in a storage higher in rank than the intermediate-rank storage, and there can be achieved a data transfer from the ES to a hierarchical storage made similarly as the data transfer from a processor to the hierarchical storage.

Further provided is control means which, following a data transfer between the hierarchical storages and ES, invalidates or retards the transferred data in the intermediate-rank storage and storages excluding MS lower in rank than the intermediate-rank storage (intermediate/lower ranking storages). More specifically, if the WS has a copy of data to be cancelled which is already in the MS destination attributable to the transfer from ES to MS, it is cancelled. If the WS does not have a copy of data of MS destination to be cancelled, which case is not a normal store-in operation, an operation to copy the data into the WS is retarded, namely it is not made valid. The discrimination between "valid" and "invalid" can be made using flag means.

With a data transfer path being provided between the intermediate-rank storage or WS and ES, when data is transferred from the MS or WS among hierarchical storages to the ES, the intermediate-rank storage is first referenced and, if the WS has a copy of the data to be transferred, the data is read out of the intermediate-rank storage and transferred to the ES, or, if the WS does not have the copy, the data is read out of the MS and transferred to the ES. Since storages higher in rank than the intermediate storage or BS are controlled in store-through mode, the transfer data read out as described above is always in the latest version among the WS and the BS.

With the control means of invalidating or retarding the copy of data to be transferred from the intermediate-storage being activated, if there is a copy of transfer data, each storage within the intermediate-rank storage which has been referenced at reading of the transfer data invalidates the copy after the data has been read out, or, if the copy is absent, retards the copy in the self storage of the data read out from a lower-rank storage.

In this way, with the control means being activated, when data transfer takes place between hierarchical storages and ES, the intermediate-rank storage can be placed in a state of having no copy of the transfer data, and accordingly for a data transfer of less urgency the control means is activated so that the intermediate storage can be used more efficiently. For an urgent data transfer between the ES and hierarchical storages, the transfer is accompanied by copying by holding the

generation of the command which activates the control means.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a data processing system provided with the extended storage system according to the invention;

Fig. 2 is a block diagram showing the arrangement of the ES 6 in Fig. 1;

Fig. 3 is a block diagram showing the arrangement of the transfer command controller 61 in Fig. 2;

Fig. 4 is a block diagram showing the arrangement of the transfer command register 611 in Fig. 3;

Fig. 5 is a block diagram showing the arrangement of the requester 62 in Fig. 2;

Fig. 6 is a block diagram showing the arrangement of the requester 63 in Fig. 2;

Fig. 7 is a block diagram showing the arrangement of the data buffer 64 in Fig. 2; and

Fig. 8 is a block diagram showing the arrangement of the WS 4 in Fig. 1.

DESCRIPTION OF THE PREFERRED EMBODIMENT

An embodiment of the inventive extended storage system will be described in detail with reference to the drawings.

In Fig. 1, the inventive extended storage system comprising hierarchical storages including, from higher to lower ranks, a buffer storage (BS) 3, a work storage (WS) 4 and a main storage (MS) 5, and an extended storage (ES) 6, with a data transfer path 70 being provided between the WS 4 and ES 6. The BS 3 and WS 4 are controlled in store-through mode and store-in mode, respectively. An instruction processor (IP) 1 and input/output processor (IOP) 2 dictate and control the data transfer between the WS 4 and ES 6 using an IP control signal line 80 and IOP control signal line 81, respectively.

The ES 6 comprises an extended storage device (will be termed ESD) 65 which stores data from the WS 4, a transfer controller 61 which controls the transfer commands from the IP 1 and IOP 2, requesters 62 and 63 which issue write requests and read requests to the WS 4 and ESD 65, and a data buffer 64 which temporarily holds data from the WS 4 and ESD 65.

The transfer controller 61 comprises, as shown in Fig. 3, transfer command registers 611 and 612 which hold and control the transfer commands from the IP 1 and IOP 2, a selector 613 which selects

the output of the transfer command register 611 or 12, and a transfer controller 614 which generally controls data transfer.

The transfer command register 611 comprise, as shown in Fig. 4, a command register 6111, a transfer volume register 6112, an MS address register 6113, an ES address register 6114, a subtracter 6115, adders 6116 and 6117, and a transfer end tester 6118 which detects that the transfer volume register 6112 becomes "empty". The transfer command register 612 has the same arrangement as 611.

Commands of data transfer between WS 4 and ES 6 are sent to the ES 6 over the transfer command lines 801 and 811, respectively, depending on the operand of each command and the contents of a general-purpose register specified by command for a command from the IP 1, or depending on the channel command word (CCW) for a command from the IOP 2. The command contains the transfer direction between the WS 4 and ES 6, the specification of activation for the control means of copy invalidation/retardation to the WS 4, the MS address and ES address indicative of the starting addresses of the transfer source and transfer destination.

Commands sent from the IP 1 are set in the respective registers 6111-6114 in the transfer command register 611, while command sent from the IOP 2 are set in the respective registers in the transfer command register 612. A command set in the transfer command register 611 or 612 is delivered to the transfer controller 614 over command line 6104 or 6105. The transfer controller 614 selects one of the command sources based on the prescribed rule and operates on the selector 613 to distribute the transfer end signal 6108, MS address 6122 and ES address 6132 from the selected transfer command register to the respective blocks so that the transfer operation is executed in accordance with the contents of the selected transfer command register.

Initially, the transfer controller 614 tests the transfer end signal 6108 and, if it is "1" indicative of "zero transfer remainder", indicates the end of transfer to the originating processor over the line 802 or 812. If, on the other hand, the transfer end signal 6108 is "0", the controller 614 analyzes the selected command and activates the requesters 62 and 63 and data buffer 64 using the command lines 6121, 6131 and 6141. The command line 6121 carries such information as transfer direction and copy control, and command lines 6131 and 6141 carry information for specifying the transfer direction and the like. In response to the activation, the selector 613 delivers the MS address to the requester 62 over the line 6122 and the ES address to the requester 63 over the line 6132.

Following the activation of the requesters 62 and 63 and data buffer 64, the transfer controller 614 directs the transfer command register over the line 6101 or 6102 to increment the MS address and ES address and decrement the transfer remainder. For example, when the command from the IP 1 is selected, the transfer controller 614 instructs the transfer command register 611 over the line 6101. On receiving the instruction, the transfer command register 611 operates on the subtracter 6115 and adders 6116 and 6117 to decrement the contents of the transfer remainder register 6112 and increment the contents of the MS address register 6113 and ES address register 6114, each by one.

The requester 62 comprises, as shown in Fig. 5, an MS address register 621 and an MS request controller 622. Similarly, the requester 63 comprises, as shown in Fig. 6, an ES address register 631 and ES request controller 632. The requesters 62 and 63 execute the transfer of 256-byte data by being activated by the transfer controller 614. In response to the activation, the MS requester 62 sets in the register 621 and MS address sent from the selector 613, and operates on its MS request controller 622 to analyze the command from the transfer controller 614. Similarly, the ES requester 63 sets the ES address in the register 631, and operates on its ES request controller 632 to analyze the command.

The data buffer 64 comprises, as shown in Fig. 7, a buffer quantity register 641, an adder/subtractor 642, a buffer quantity controller 643 which controls the requesters 62 and 63 depending on the quantity of buffer, and a buffer 644 which temporarily holds transferred data. By being activated by the transfer command controller 61, the data buffer 64 recognizes the data transfer direction based on the command sent over the line 6141. The buffer quantity controller 643 controls the requesters 62 and 63 using the lines 6421 and 6431 so that the data transfer source prevents the overflow of buffer 644 when its contents reach a certain level and the data transfer destination holds the issuance of request until a certain amount of data is stacked in the buffer 644. The above-mentioned certain level of buffer is controlled depending on the data transfer direction.

The requester 62 responds to the activation by the transfer controller 614 to send immediately, in case of the data transfer source being MS (accordingly, the destination is ES), the command from the MS request controller 622 together with the MS address in the register 621 to the WS over the line 7011, and issues a read request. The requester 63 holds the issuance of request to the ESD 65 until it is informed by the buffer 64 over the line 6431 that a specified amount of data is stacked in the buffer 644. The data buffer 64, when

readout data is sent from the WS 4 over the line 7042 in response to the read request, writes the readout data in the buffer 644, with an acknowledgement sent over the line 703 in synchronism with the data being a buffer write request. At this time, the adder/subtractor 642 increments the buffer quantity register 641 by one. The buffer quantity controller 643 examines the contents of the updated buffer quantity register 641 to judge whether the specified amount of data is stacked in the buffer 644. The buffer 64 repeats the above operations at each reception of readout data.

When the specified amount of data has been stacked in the buffer 644, the buffer quantity controller 643 indicates it to the requester 63 over the line 6431. In response to this signal, the requester 63 issues a buffer read request to the buffer over the line 6431, sends the command from the ES request controller 632 together with the ES address in the register 631 to the ESD 65, and issues a write request. At this time, the buffer 64 responds to the buffer read request of the requester 63 to read out the transfer data from the buffer 644 and sends it as write data to the ESD 65 over the line 7061. At the same time, the adder/subtractor 642 subtracts by 32 the contents of buffer quantity register 641. The subtrahend "32" is determined on the basis that the write request to the buffer 644 is 8-byte units, whereas the read request is 256-byte units, i.e., 32 fold.

In case of the data transfer source being ES (accordingly, the destination is MS), the requester 63 responds to the activation by the transfer controller 614 to send immediately the ES address and command to the ESD 65, and issues a read request. The requester 62 holds the issuance of request to the WS 4 until it is informed by the buffer 64 over the line 6421 that a specified amount of data is stacked in the buffer 644. The data buffer 64, when readout data is sent from the ESD 65 over the line 7062 in response to the read request, writes the readout data in the buffer 644, with an acknowledgement sent over the line 653 in synchronism with the data being a buffer write request. The buffer quantity register 641 has its contents incremented by one, and the buffer quantity controller 643 examines whether the specified amount of data is stacked in the buffer 644.

When the specified amount of data has been stacked in the buffer 644, the buffer quantity controller 643 indicates it to the requester 62 over the line 6421. In response to this signal, the requester 62 issues a buffer read request to the buffer over the line 6241, sends the MS address and command to the WS 4, and issues a write request. At this time, the buffer 64 responds to the buffer read request of the requester 62 to read out the transfer data from the buffer 644 and sends it as write data

to the WS over the line 7041. At the same time, the adder/subtractor 642 subtracts by 32 the contents of buffer quantity register 641.

In response to the delivery of the termination of requests from the WS 4 and ESD 65 to the requesters 62 and 64 over the lines 702 and 652, respectively, the requesters 62 and 63 indicate the end of data transfers, which have been initiated by the transfer controller 614, to the transfer controller 614 over the lines 6211 and 6311. Receiving the termination signals from both requesters 62 and 63, the transfer controller 614 tests the transfer end on the line 6108 from the selector 613, and, if it is "1" indicative of zero transfer remainder, indicates it to the originating processor over the line 802 or 812. If the line 6108 is "0", the transfer controller 614 activates the requesters 62 and 63 and buffer 64 to execute the data transfer by following the foregoing procedure.

Next, the operation of the WS 4 upon receiving a request from the requester 62 will be described. The WS 4 comprises, as shown in Fig. 8, a command controller 41, an address controller 42, a write data controller 43, a work storage address controller 44, a work storage device 45 (will be termed WSD), an MS requester 46, a buffer memory cancellation controller 47, and a readout data controller 48. The WS 4 has a pair of data transfer paths for IP 1 and IOP 2, as in the conventional system, which is added by the third data transfer path for the ES 6, so that it can deal with requests from ES 6 as well as those from the IP 1 and IOP 2.

When the ES 6 issues a request to the WS 4, the WS 4 shown in Fig. 8 sets the command and MS address sent from the requester 62 over the lines 7011 and 7012 in the command controller 41 and address controller 42, respectively. For a write request, write data from the data buffer 64 is further entered to the data controller 43 over the line 7041. The command from the ES 6 entered in the command controller 41 is added to commands from the IP 1 and IOP 2 for selection based on the prescribed rule. If the command from the ES 6 is selected, the WS 4 processes the request from the ES 6 in accordance with this command, the MS address from the requester 62 entered in the address controller 42 and write data from the data buffer 64 entered in the write data controller 43 at the time of write request. The WS 4 is assumed to make a copy of MS in a 256-byte unit and generate a request to the MS 5 in a 256-byte unit.

The WS 4, in case of the request from ES 6 being a read request, first enters the MS address 421 in the work address controller 44 to examine whether it has a copy of data of the MS address. If the data is found copied, the work storage address controller 44 reads out the data from the WSD 45

over the line 441. At this time, the address of the WSD 45 is part of the MS address 421 and on the line 442 for the rest. The data 451 read out of the WSD 45 is sent, together with the acknowledgement from the readout data controller 48 onto the line 703, to the data buffer 64 over the line 7042. In case the line 411 indicates that the invalidation or retardation of copy of the data is specified by the command, the work storage address controller 44, after the above-mentioned examination of copy, resets the copy valid bit to "0".

The work storage address controller 44, if data of the MS address is not copied, operates on the MS requester 46 over the line 441 to issue a read request to the MS 5. In this case, the MS address 421 is used. The MS requester 46 sends the command and MS address to the MS 5 over the lines 4501 and 4502, and issues a read request. The MS 5 responds to the read request to send back readout data and acknowledgement in synchronism with the data. Then, the work storage address controller 44 makes a new copy of the data as data of the MS address, and the readout data controller 48 sends the data to the data buffer 64 over the line 7042, while at the same time making acknowledgement to the line 703. At this stage of copying, the work storage address controller 44 gets a new storage location in the WSD 45 in accordance with the widely-known LRU (Least Recently Used) algorithm, and writes the readout data 5402 on the line 441 into the WSD 45. The address of WSD 45 indicative of the newly established storage location is given as part of the MS address 421 and on the line 442 for the rest. However, in case the line 411 indicates that the invalidation or retardation of the copy of the data is specified by the command, the work storage address controller 44 does not make the copy, and accordingly does not execute the writing to the WSD 45.

Next, the operation of the WS 4, in case of the request from the ES 6 being a write request, will be described. Initially, the WS 4 enters the MS address 421 to the work storage address controller 44 to examine whether data of the MS address is copied. If the data is copied, the work storage address controller 44 writes write data 431 into the WSD 45 over the line 441. Also in this case, the address of the WSD 45 is given as part of the MS address 421 and the line 442. If the line 411 indicates that the invalidation or retardation of the copy of the data is specified by the command, the work storage address controller 44 resets the copy valid bit to "0", and operates on the MS requester 46 over the line 441 to issue a write request to the MS 5, instead of writing the write data 431 into the WSD 45. In this operation, the MS address 421 and write data 431 are used. The MS requester 46 sends the command, MS address and write data to

the MS 5 over the lines 4501, 4502 and 4503, and issues a write request.

If data of the MS address is not copied, the work storage address controller 44 makes a new copy of the write data 431 as data of the MS address, and writes the data 431 over the line 441 into a storage location established newly in the WSD 45 in the same manner as the previous case. In this operation, the address of WSD 45 indicative of the new storage location is given as part of the MS address and line 442 for the rest. However, in case the line 411 indicates that the invalidation or retardation of the copy of the data is specified by the command, the work storage address controller 44 does not make the copy, and operates on the MS requester 46 over the line 441 to issue a write request to the MS 5, as in the previous case, instead of writing the write data 431 into the WSD 45.

In case of the request from the ES 6 being a write request, the WS 4 further examines with the buffer memory cancellation controller 47 the state of copy of data of the MS address to the BS 3 in parallel to the copy examination for the data to the WS 4 by the work storage address controller 44. The buffer memory cancellation controller 47 is provided in advance with a front buffer address array (FAA) which stores the copy state of BS 3. In this case, the MS address 421 is entered to the controller 47 to examine whether data of the MS address is copied in the BS 3. If the data is found copied, the buffer memory cancellation controller 47 requests to the IP 1 over the line 4101 the cancellation of copy of the MS address indicated on the line 4102, thereby preventing the data written in the WSD 45 or MS 5 from becoming much newer than the data copied in the BS 3.

Although in the foregoing embodiment of this invention, the hierarchical storage system is organized in three ranks of BS 3, WS 4 and MS 5, the invention is also applicable to the system which further includes a storage of another rank controlled in store-in mode located between the WS 4 and MS 5, or a storage controlled in store-through mode located between the BS 3 and WS 4.

Claims

1. An extended storage system comprising:
 - (a) an instruction processor (1, 2);
 - (b) a main storage (5) connected to said instruction processor;
 - (c) a buffer storage (3) which is connected to said instruction processor, holds part of said main storage and has a function of being accessed faster than said main storage;

(d) at least one work storage (4) which is connected between said main storage and said buffer storage and has a function of being accessed at an intermediate access speed between access speeds of said main storage and buffer storage, said buffer storage being controlled in store-through mode for said work storage, said work storage being controlled in store-in mode for said main storage; and

(e) an extended storage (6) which is connected to said work storage through a transfer path and has a storage capacity for supplementing the storage capacity of said main storage, said extended storage having an address space which is different from the address space of said main storage.

2. An extended storage system according to claim 1 further comprising:

valid flag means (44) which is provided for said work storage and adapted to indicate the validity of part of said main storage held in said work storage; and

a command controller (41) which issues to said flag means a signal (411) indicative of the validity of data in said work storage related to data to be transferred, in accordance with a transfer command for said extended storage issued by said instruction processor.

3. An extended storage system according to claim 2 further comprising:

a buffer storage cancellation controller (47) which is connected to said command controller and adapted to control the cancellation of part of data in said buffer storage; and

a buffer address array (BAA) which is provided in said buffer storage and adapted to control the validity of a copy, from said main storage, of data corresponding to part of address in said buffer storage, on the basis of the output of said buffer storage cancellation controller provided in said buffer storage.

4. An extended storage system according to claim 2, wherein said extended storage comprises: means (6111-6114) of holding the number of words of data transferred to/from said work storage over said transfer path, the starting address of said extended storage, the starting address of said main storage and said transfer command; and means (6115-6117) of updating said starting addresses and said number of words at a transfer to/from said extended storage.

5. An extended storage system for a data processing system which comprises an instruction processor (1), an input/output processor (2) and hierarchical storages of three ranks or more (3, 4, 5), with an intermediate-rank storage among said hierarchical storages being controlled for storing in

store-in mode, wherein said extended storage system comprises:

an extended storage (6); and

a data transfer path (70) provided between said intermediate-rank storage and said extended storage for implementing data transfer between said hierarchical storages and said extended storage in accordance with a command from said instruction processor or said input/output processor.

6. An extended storage system according to claim 5, wherein in transferring data from said extended storage in said hierarchical storages, a copy of data corresponding to the transfer destination of said data to be transferred among data copied in a storage higher in rank than said intermediate-rank storage is invalidated.

7. An extended storage system according to claim 5, wherein in transferring data between said hierarchical storages and said extended storage, copies of said data to be transferred in said intermediate-rank storage are invalidated or retarded.

FIG. 1

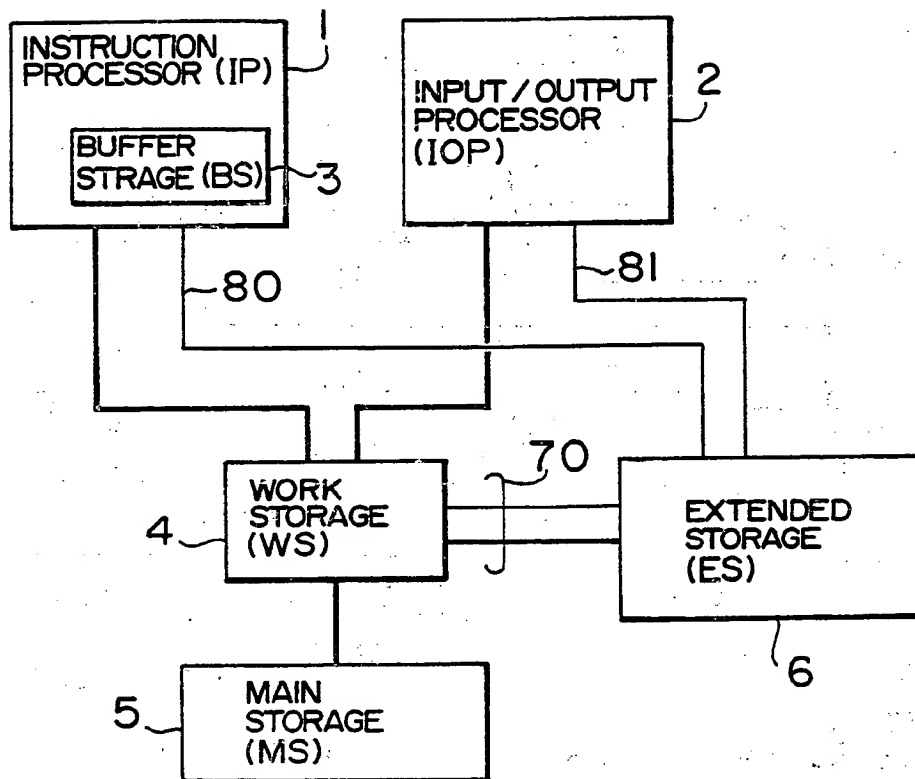


FIG. 2

EXTENDED STORAGE

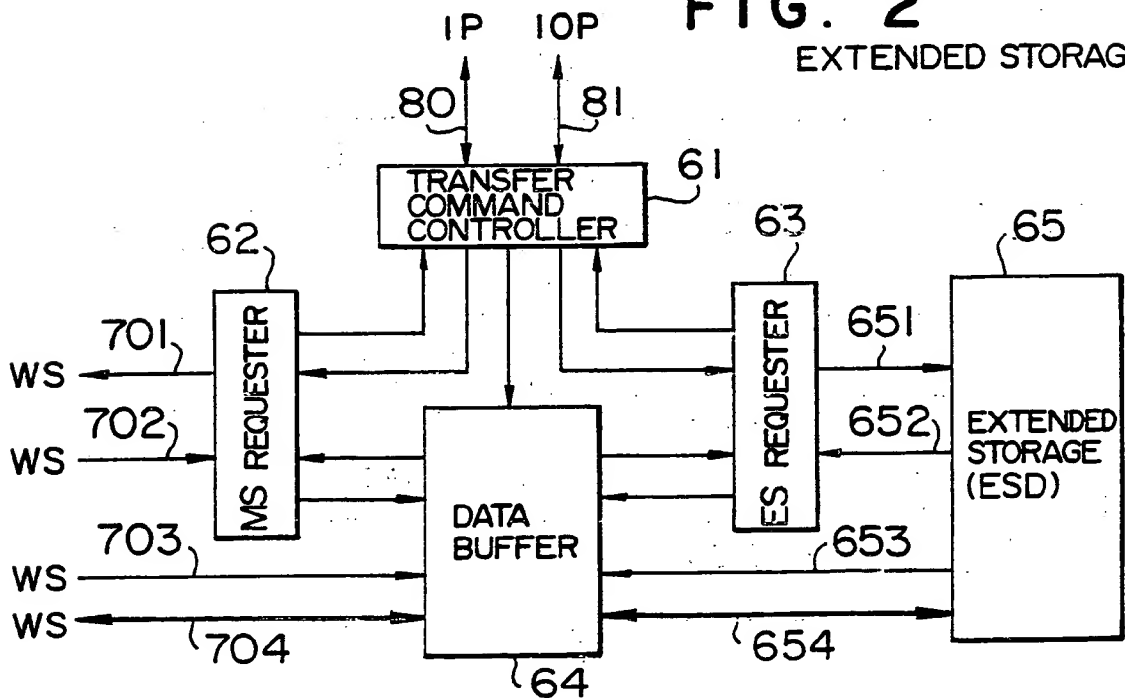


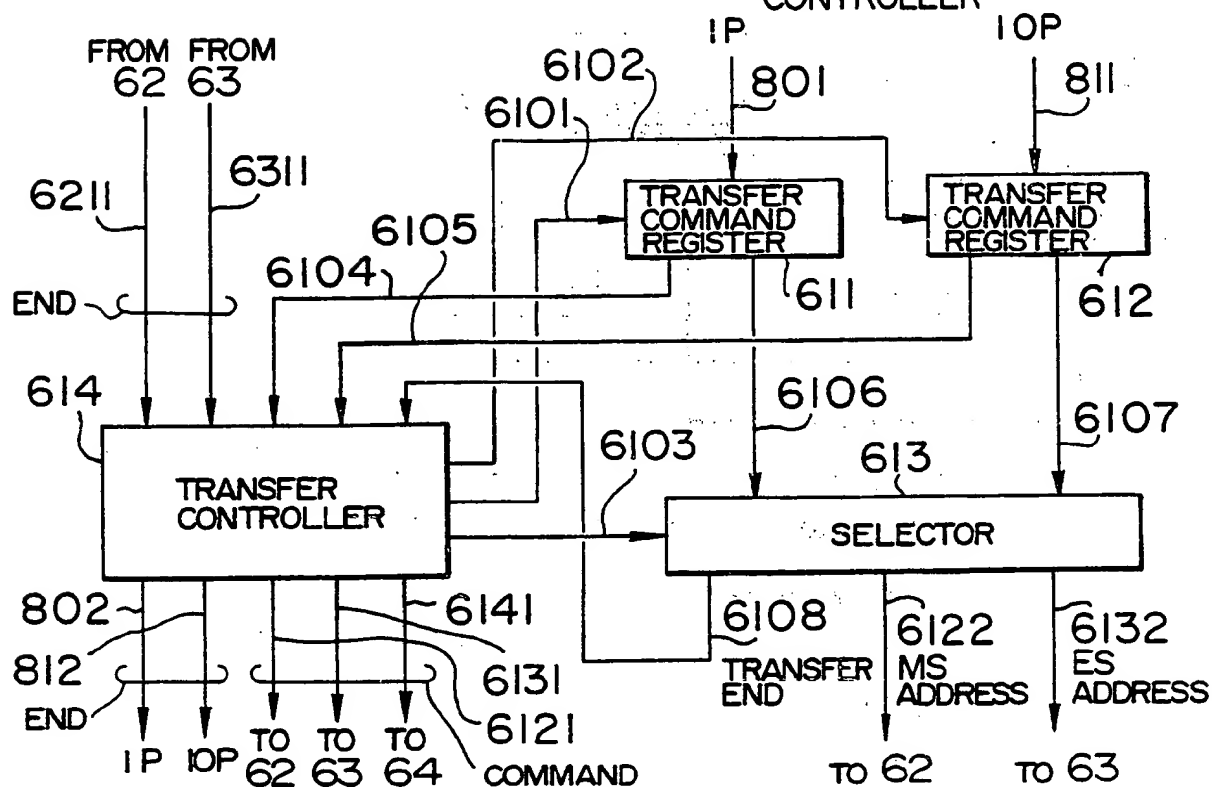
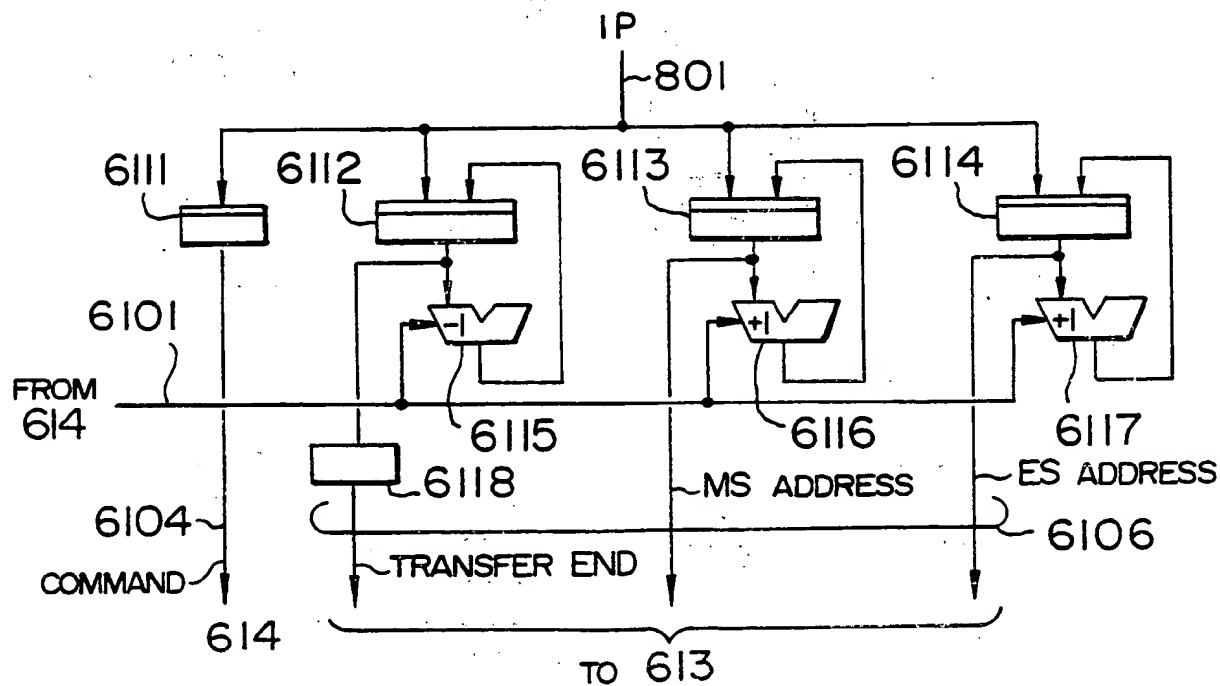
FIG. 3 TRANSFER COMMAND CONTROLLER**FIG. 4** TRANSFER COMMAND REGISTER

FIG. 5 REQUESTER 62

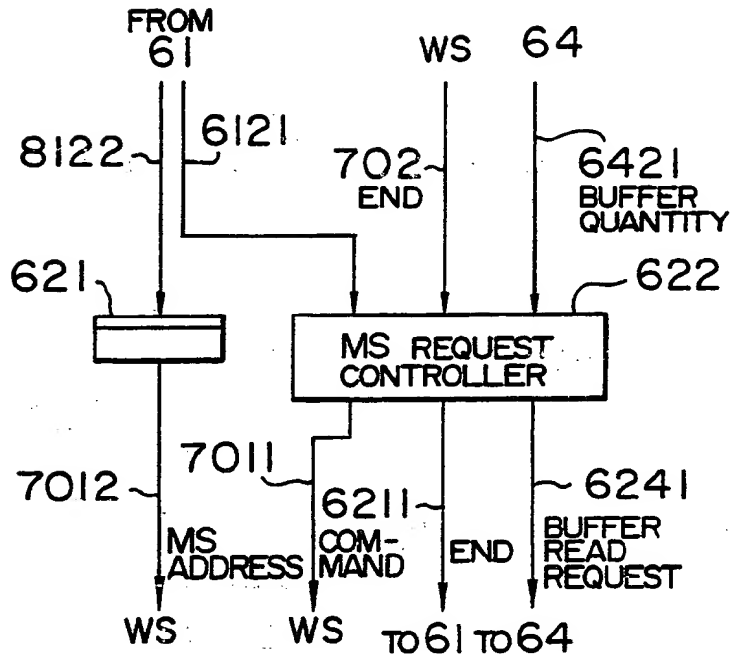


FIG. 6 REQUESTER 63

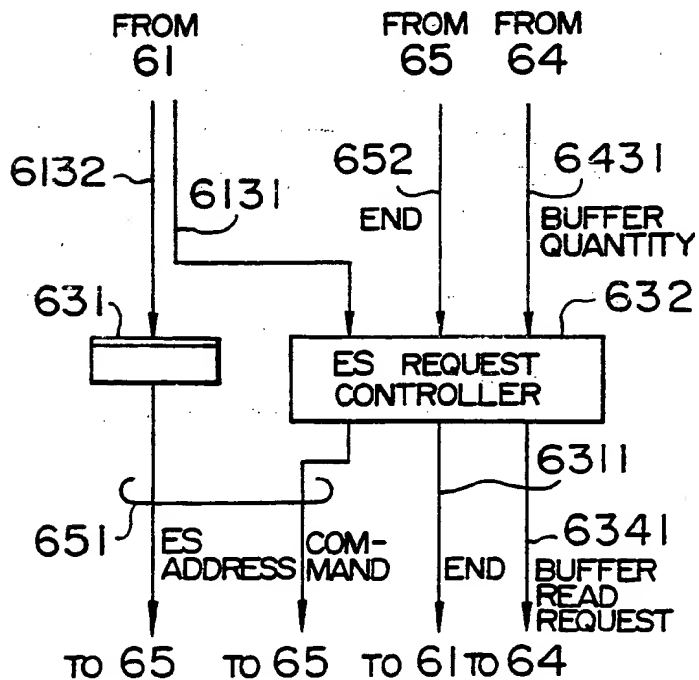


FIG. 7 DATA BUFFER

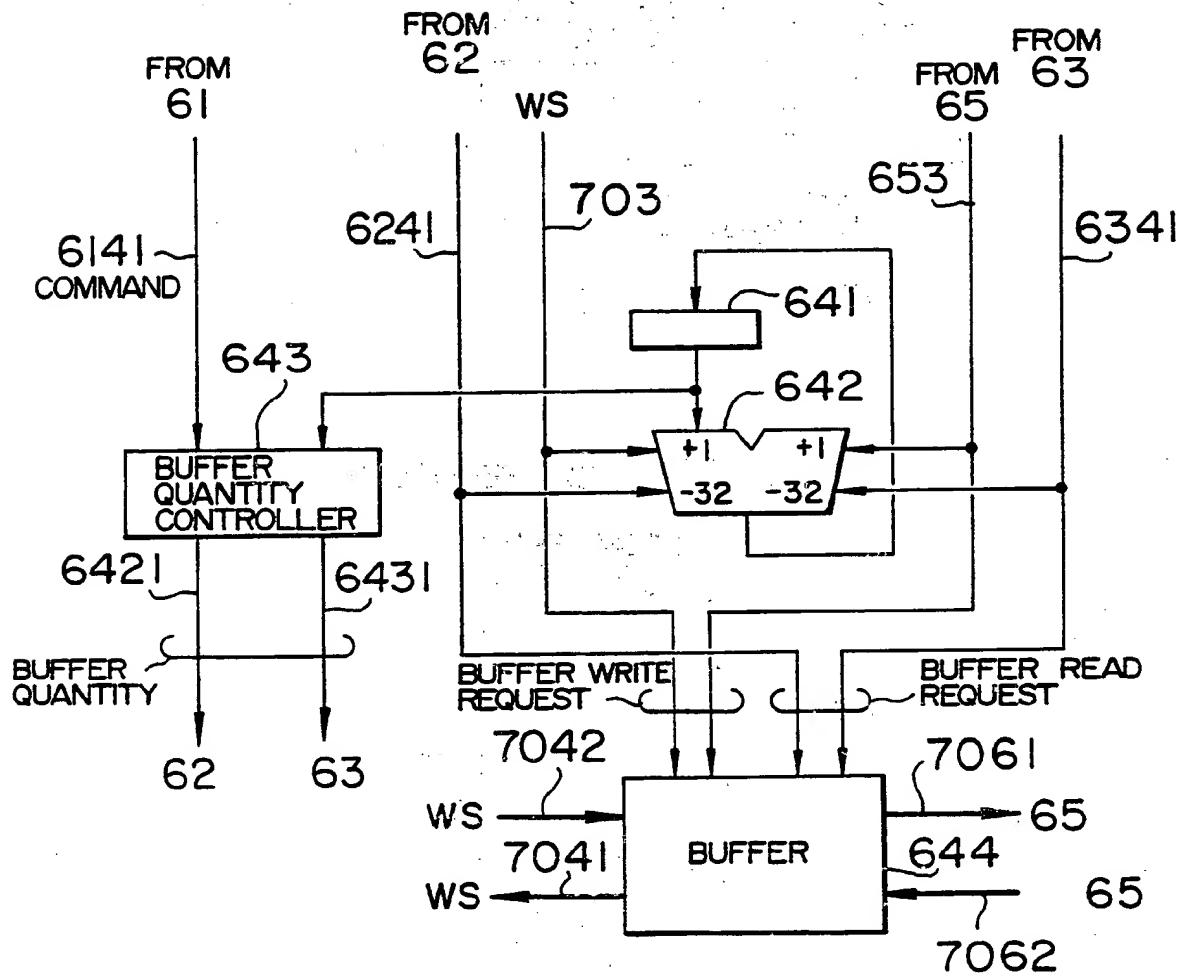
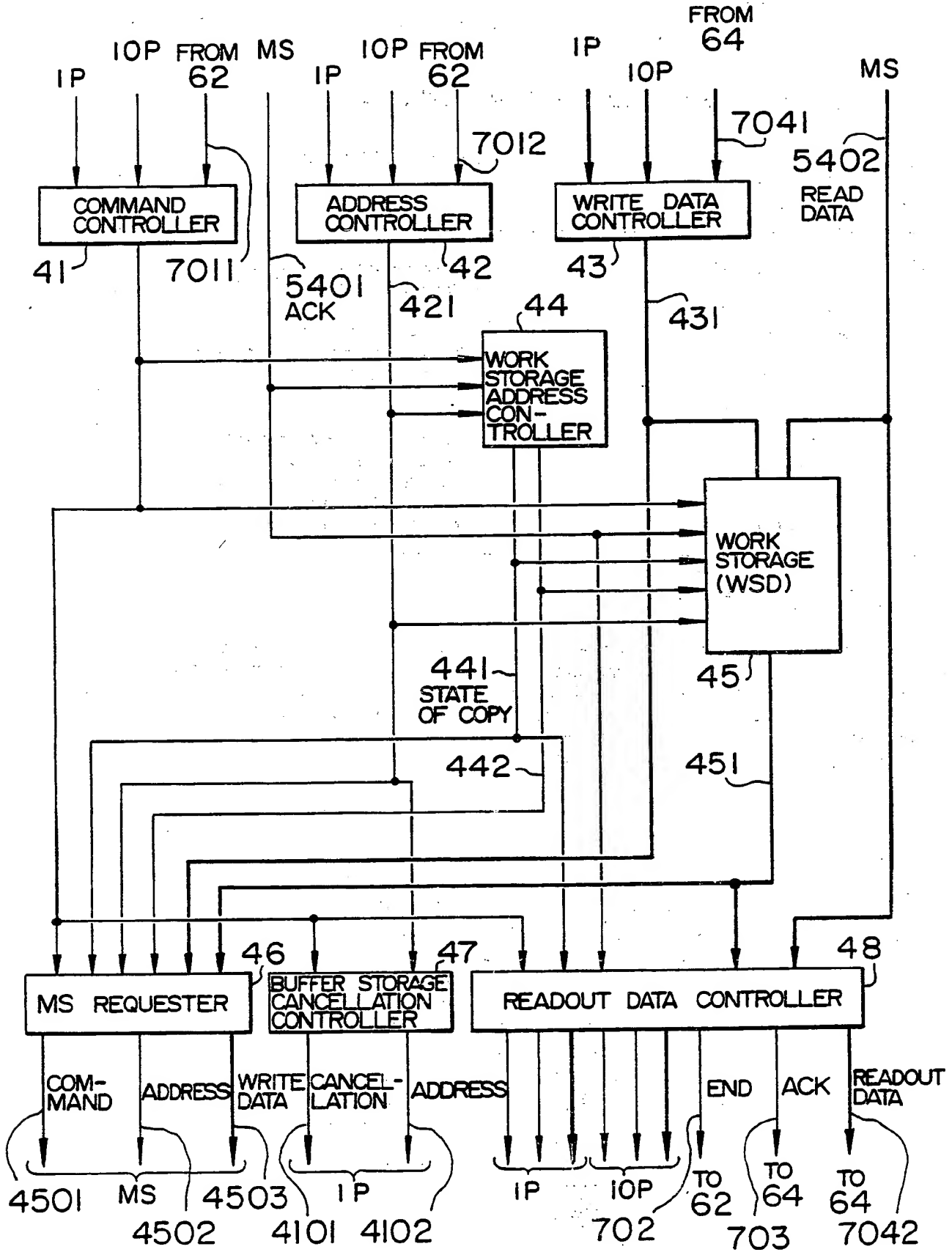


FIG. 8 WORK STORAGE



(19)



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(71) Applicant: **HITACHI, LTD.**

**6, Kanda Surugadai 4-chome
Chiyoda-ku, Tokyo 101(JP)**

(72) Inventor: **Kiri, Yoshio
2-2-501, Minamigaoka-2-chome
Hadano-shi(JP)**

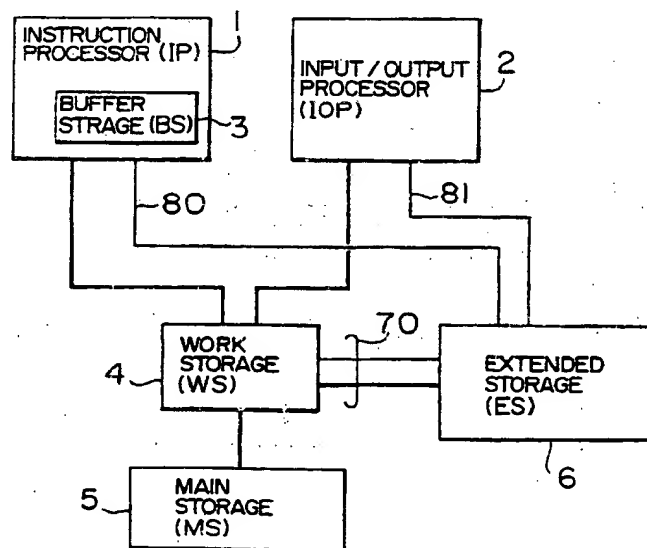
(74) Representative: **Patentanwälte Beetz sen. -
Beetz jun. Timpe - Siegfried -
Schmitt-Fumian- Mayr
Steinsdorfstrasse 10
W-8000 München 22(DE)**

(54) **Extended storage system.**

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of a copy of data, in part pertinent to the data transfer destination, in accordance with the transfer command which specifies invalidation or retardation of the copy from the main storage.

FIG. 1





European
Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 89 10 2752

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y	EP-A-0 214 870 (FUJITSU) * Column 1, lines 29-42; column 2, lines 7-37; column 3, lines 1-27; column 4, lines 16-31; column 6, line 50 - column 7, line 28; figures 1,2 *	1,2,5-7	G 06 F 12/08
A		3,4	
Y	EP-A-0 173 893 (IBM) * Page 1, lines 22,23; page 3, lines 9-15; page 7, lines 6-20; page 8, lines 13-21; page 12, line 29 - page 13, line 5; figure 1 *	1,2,5-7	
A		3,4	
Y	EP-A-0 165 823 (FUJITSU) * Page 2, line 27 - page 3, line 23; page 5, line 26 - page 9, line 5 *	2,6,7	
A		1,3-5	
A	PROCEEDINGS OF THE IFIP 9TH WORLD COMPUTER CONGRESS, Paris, 19th - 23rd September 1983, pages 693-697, North-Holland, Amsterdam, NL; A. HATTORI et al.: "Three-level hierarchical storage system for FACOM M-380/382" * Page 693, left-hand column, line 26 - page 695, left-hand column, line 8 *	1,5	
The present search report has been drawn up for all claims			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			G 06 F 12/00
Place of search The Hague		Date of completion of search 19 February 91	Examiner MASCHE C.M.
CATEGORY OF CITED DOCUMENTS X: particularly relevant if taken alone Y: particularly relevant if combined with another document of the same category A: technological background D: non-written disclosure P: intermediate document T: theory or principle underlying the invention E: earlier patent document, but published on, or after the filing date D: document cited in the application L: document cited for other reasons &: member of the same patent family, corresponding document			

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